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Capacitor Voltages Measurement and Balancing in Flying Capacitor Multilevel Converters Utilizing a Single Voltage Sensor

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***Abstract*—This paper proposes a new method for measuring capacitor voltages in multilevel flying capacitor (FC) converters that requires only one voltage sensor per phase-leg. Multiple dc voltage sensors traditionally used to measure the capacitor voltages are replaced with a single voltage sensor at the ac-side of the phase-leg. The proposed method is subsequently used to balance the capacitor voltages using only the measured ac voltage. The operation of the proposed measurement and balancing method is independent of the number of the converter levels. Experimental results presented for a five-level FC converter verify effective operation of the proposed method.**

I. Introduction

MULTILEVEL converters have attracted significant interest for medium/high power applications [1]–[3]. Among various multilevel converter topologies [4], the flying capacitor (FC) converter is one of the popular structures [5]–[10]. The FC converter [11] offers some advantages over the neutral-point-clamped (NPC) converter [12], such as that capacitor voltage balance can be achieved without producing low frequency voltage ripples in the FCs, even in converters with a large number of levels.

Phase-shifted pulse-width modulation (PS-PWM) is a common technique applied to FC converters, as it provides natural capacitor voltage balance [21]. However, the quality of line-to-line voltages is not the best [13]. On the other hand, phase-disposition PWM (PD-PWM) produces better line-to-line voltages than PS-PWM, but it cannot be applied straightforward to the FC converter. Some solutions to produce PD-PWM are based on modifying the shapes of the carriers [14], [15]. However, each cell requires different carriers, which complicates its practical implementation, especially for FC converters with a large number of levels. The technique was simplified in [16], and the number of carriers was reduced from $(n-1)^2$ to $(n-1)$, n being the number of voltage levels. The main drawback is that it requires significant digital signal power processing. A similar kind of technique was proposed in [20] with the advantage of using only a single carrier.

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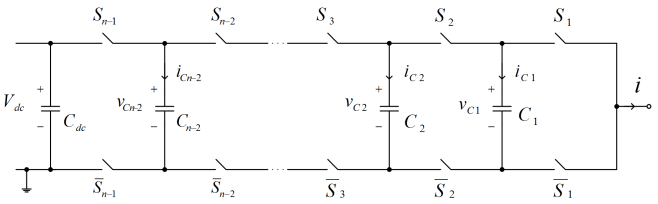

Fig. 1. Phase-leg of an n-level FLC Converter.

The property of natural capacitor voltage balance in FC converters can be boosted by the addition of RLC filters connected to the output of the converter [17]–[20]. Closed-loop voltage balancing methods have also been reported in the technical literature [22]–[28]. However, the main disadvantage in those techniques is the use of multiple voltage sensors (one sensor per capacitor), which increases the system complexity and reduces reliability.

This paper proposes a new capacitor voltage measuring method that requires a single voltage sensor per phase-leg. The proposed measuring method is used to improve the balancing method discussed in [27] for multilevel FC converters. The proposed balancing method is simpler than the conventional one (based on using multiple voltage sensors) and requires only one voltage sensor. As in [27], the proposed method is able to maintain capacitor voltage balance and is very simple to implement in a digital signal processor.

The paper is organized as follows. Section II describes the operating principle of a FC converter and the PS-PWM technique. Section III introduces the proposed capacitor voltages measurement and balancing method based on a single sensor. Section IV presents experimental results obtained from a single-phase five-level FC converter. Finally, the conclusions are summarized in Section V.

II. FC Converter and PS-PWM

A. Fundamentals

Fig. 1 shows a phase-leg of an n-level FC converter, which integrates n-2 FCs. The switch pairs in the phase-leg $s_1-\bar{s}_1$, $s_2-\bar{s}_2$,..., and $s_{n-1}-\bar{s}_{n-1}$ operate in a complementary

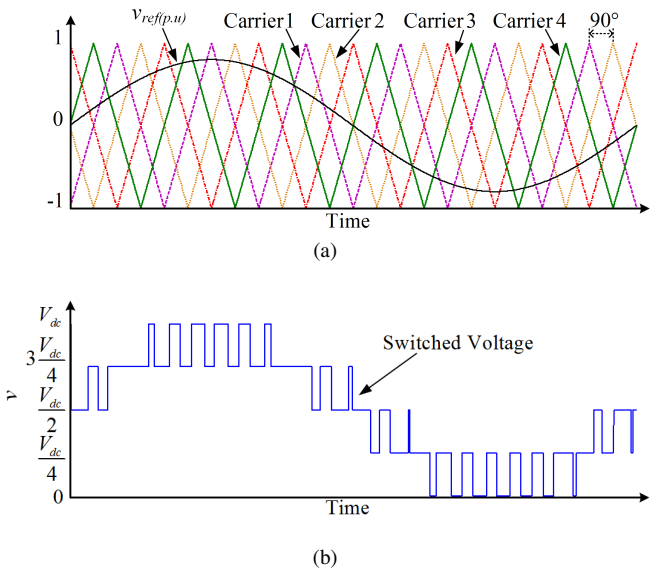

Fig. 2. PS-PWM technique for a five-level converter: (a) reference sinusoidal signal with four triangular carriers and (b) switched phase voltage.

manner. During normal operation, the mean voltage values of the FCs, C_1, C_2,..., and C_{n-2}, should be maintained at $V_{dc}/(n-1)$, $2V_{dc}/(n-1)$,..., and $(n-2)V_{dc}/(n-1)$, respectively, where V_{dc} is the dc-bus voltage. Consequently, the voltage across each switch is only $1/(n-1)$ of the dc-bus voltage. Each converter's phase-leg can generate n output voltage levels, i.e., 0, $V_{dc}/(n-1)$, $2V_{dc}/(n-1)$,..., $(n-2)V_{dc}/(n-1)$, and V_{dc}, with respect to the dc negative rail "0". Using Kirchhoff's voltage and current laws, the line-to-ground voltage, v, and the currents through the FCs can be written as:

$$v = s_{n-1}V_{dc} + \sum_{j=1}^{n-2} v_{cj}(s_j - s_{(j+1)}) \tag{1}$$

$$i_{Cj} = (s_{j+1} - s_j)i, \tag{2}$$

for $j = \{1, 2, ..., n-2\}$.

The control functions s represent the states of the upper switches, which take the values 0 or 1 when the corresponding switch is off or on, respectively.

B. PS-PWM Technique

Fig. 2 shows the reference and carrier signals using a PS-PWM scheme applied to a five-level converter. In this converter, PS-PWM requires four carriers of the same amplitude and frequency, with a 90° phase-shift between consecutive carriers. A sinusoidal reference signal (v_{ref}) that ranges in the interval [-1, 1] under the linear modulation mode, is compared with all four triangular carriers to define the state of the switches. With this technique, each carrier is usually associated to a particular pair of switches. Using this method, natural voltage balancing can be achieved. However, this natural voltage balancing is usually slow and depends on the loading conditions. Therefore, an active balancing method is required to regulate the FC voltages at their desired levels with

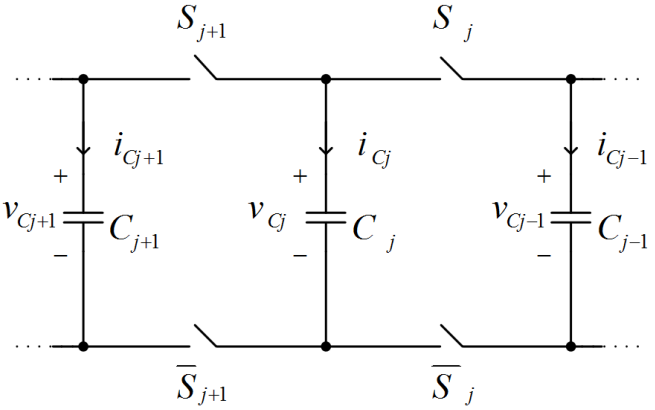

Fig. 3. A section of the FC chain.

improved dynamics, especially under transient conditions and nonlinear loads.

The active voltage balancing method developed in [27], is based on the analysis of a generic cell section of the FC converter, as shown in Fig. 3. According to (2), the current through a capacitor is affected by the control signals associated with the two adjacent switches. The locally-averaged representation of the capacitor current in (2) calculated over a switching period is:

$$\bar{i}_{Cj} = (d_{j+1} - d_j)\bar{i}, \tag{3}$$

where $\bar{i}_{Cj}$ and $\bar{i}$ are the locally-averaged currents of the capacitor C_j and the output current, respectively, and d_{j+1} and d_j are the duty cycles of the switches s_{j+1} and s_j, respectively.

Assuming positive output current ($i > 0$), (3) shows that increasing the duty cycle d_{j+1} will increase the locally-averaged current through the capacitor, whereas the opposite effect will be produced if d_j is increased. If the voltage of the capacitor C_j is greater than its reference value, a negative current should be imposed to this capacitor. Therefore, the duty cycles d_j and d_{j+1} should be increased and decreased, respectively. On the other hand, if the output current is negative ($i<0$), the duty cycles should be manipulated in the opposite direction to help for voltage balance. Based on this analysis, the voltage balancing method shown in Fig. 4(a) was proposed in [27].

The voltage balancing dynamics of the capacitor C_j can be analyzed based on:

$$\frac{d\bar{v}_{Cj}}{dt} = \frac{\bar{i}_{Cj}}{C_j}. \tag{4}$$

From (3) and (4), one can obtain:

$$\frac{d\bar{v}_{Cj}}{dt} = \frac{\bar{i}(d_{j+1} - d_j)}{C_j}, \tag{5}$$

where,

$$d_{j+1} = d_m + \Delta d_{j+1}, \tag{6}$$

$$d_j = d_m + \Delta d_j, \tag{7}$$

where d_m ranges in the interval [0,1] and is derived as follows:

$$d_m = \frac{v_{ref(p.u)} + 1}{2}, \tag{8}$$

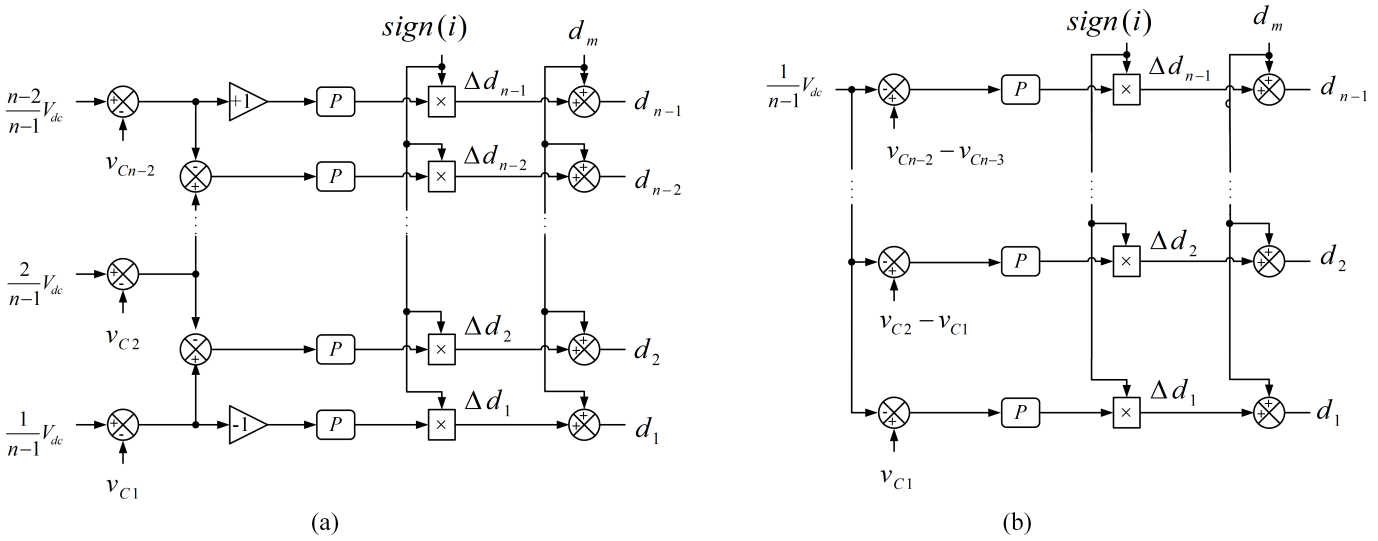

Fig. 4. a) Active voltage balancing method for a general n-level FC converter proposed in [27], b) Voltage balancing method for a general n-level FC converter proposed in this paper.

where, $v_{ref(p.u)}$ is the normalized ac reference signal within the interval [-1, 1].

Assuming small variations around the operating point, using (6) and (7) in (5), one can obtain:

$$\frac{\Delta \overline{v}_{Cj}}{\Delta t} = \frac{\overline{i}(\Delta d_{j+1} - \Delta d_j)}{C_j}. \tag{9}$$

The variations of the duty cycles are given by a proportional controller, as follows:

$$\Delta d_{j+1} = sign(i)(\varepsilon_j - \varepsilon_{j+1})P, \tag{10}$$

$$\Delta d_j = sign(i)(\varepsilon_{j-1} - \varepsilon_j)P, \tag{11}$$

where ε_{j-1}, ε_j, and ε_{j+1} are the voltage errors in the capacitors C_{j-1}, C_j, and C_{j+1}, respectively, and P is the proportional control parameter. $sign(i)$ is the sign of the output current defined as 1 and -1 when i is positive and negative, respectively. Substituting (10) and (11) into (9):

$$\frac{\Delta \overline{v}_{cj}}{\Delta t} = \frac{|\overline{i}|P(2\varepsilon_j - \varepsilon_{j+1} - \varepsilon_{j-1})}{C_j} \tag{12}$$

defines the balancing dynamic of the proposed voltage control and can be used to tune the controller gain parameter (P) to achieve a satisfactory system performance. This technique is very simple to implement on FC converters with any number of levels, as it just requires a proportional controller. However, the main drawback is the need for multiple dc voltage sensors.

III. Proposed Method for Measuring Capacitor Voltages and Performing Voltage Balancing

In this section, a method for capacitor voltages measurement and balancing in FC converters is described. The objective of the method is to measure and regulate all the capacitor voltages by only using the output voltage measurement, v. The relationship between the output voltage and the capacitor voltages is governed by the switching function shown in (1).

There are two general strategies proposed in the literature to reconstruct the capacitor voltages of multilevel converters by sensing the ac output voltage. In the first strategy, the capacitor voltages are measured directly when there is only one capacitor conducting. The shortcoming of this approach is that it fails to provide measurement for the switching instances where several capacitors contribute to build the output voltage. Therefore, the chance of measuring the capacitor voltages is limited, especially in converters with high number of levels. For the switching instances in which multiple capacitors are conducting, an estimation mechanism needs to be implemented to provide the voltage feedback signal for the controller [29].

The second strategy, on the other hand, does not rely on the direct measurement. It monitors the voltage steps on the output voltage and therefore, measures the voltage of the capacitor that produced the step. This strategy provides a measurement at each switching instance for modular converters with equal capacitor voltages such as cascaded H-bridge (CHB) converter [30], [31]. However, the shortcoming of this strategy is that it does not provide a measurement when several capacitors switch at the same time to generate the voltage step. This situation happens most of the times in the FC converter as the voltage steps are generated by simultaneous switching of two adjacent capacitors, as it can be seen from (1). Therefore, in this strategy only v_{C1}, and if V_{dc} is known, v_{n-2} as well can be measured, and the rest of the capacitor voltages need to be estimated or measured individually.

Therefore, none of the abovementioned strategies are suitable for the FC converter. The objective is to provide the converter controller with capacitor voltages measured at a constant sampling frequency. In order to achieve this goal, (1) is rewritten as:

$$v = \sum_{j=1}^{n-1} (v_{Cj} - v_{Cj-1}) s_j \tag{13}$$

with $v_{C0} = 0$ and $v_{C(n-1)} = V_{dc}$.

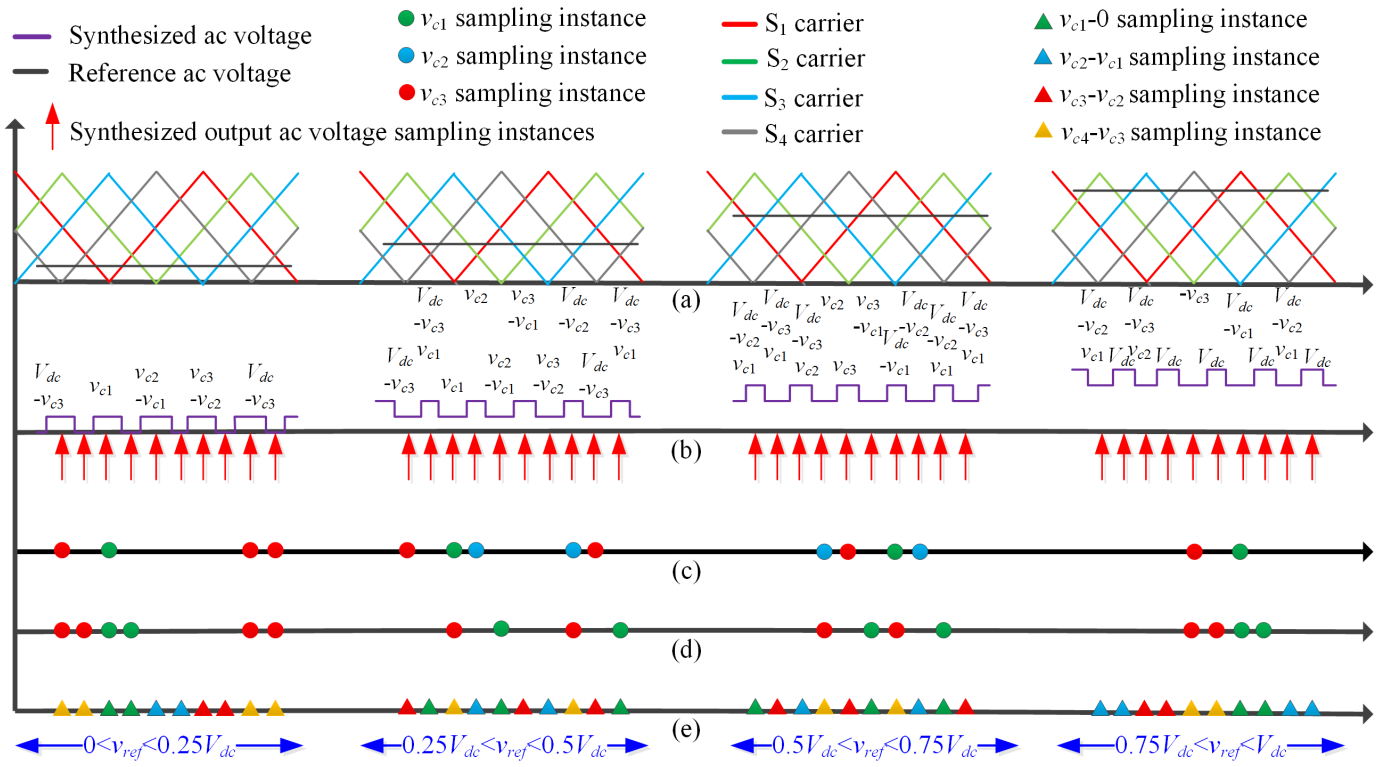

Fig. 5. (a) Carrier waveforms and reference signals for all possible voltage regions, (b) synthesized output voltage and number of conducting capacitors for each switching instance, (c) voltages sampling instances using the direct capacitor voltage measurement strategy, (d) voltages sampling instances using the indirect capacitor voltage measurement strategy, and (e) voltages sampling instances using the proposed measurement strategy.

From (13), it can be seen that after each switching instance when s_j changes, $v_{Cj} - v_{Cj-1}$ can be measured indirectly from:

$$v_{Cj} - v_{Cj-1} = |\frac{v' - v''}{s'_j - s''_j}|, \tag{14}$$

where, v' and s' are the quantities before the transition (output voltage step) and v'' and s'' are values after the transition. This is equivalent to measuring capacitor voltages in a CHB converter using the second strategy.

In this strategy the voltages on the rest of the conducting capacitors are assumed to remain constant during the time interval in between the two measurements. This assumption is generally acceptable because the elapsed time in between the two measurements is $1/(2Nf_s)$ (f_s being the carrier frequency and N the number of carriers), which remains very small in practice. Nevertheless, the effect of these voltage changes can be included in (14) to make the proposed measurement method more accurate, but at the expense of added complexity.

The active capacitors voltage balancing method discussed in Section II-B and shown in Fig. 4(a) uses the capacitor voltages as direct feedback. Using the new variables, the control system can be redrawn in a much simpler form as shown in Fig. 4(b).

Fig. 5 shows an example for a five-level converter. In this case, there are four regions where the reference signal can be located in: $0 < v_{ref} < 0.25V_{dc}$, $0.25V_{dc} < v_{ref} < 0.5V_{dc}$, $0.5V_{dc} < v_{ref} < 0.75V_{dc}$, and $0.75V_{dc} < v_{ref} < V_{dc}$. Four different examples are shown that correspond to operation in each of these voltage regions.

The triangular carriers and the reference waveform are shown in Fig. 5(a). The synthesized output voltage and the sampling instances are shown in Fig. 5(b). The inserted capacitors that generate each pulse are also indicated. The measurement instances need to be synchronised with the carriers to ensure that voltage measurements happen at the centre of each PWM pulse. Therefore, when a triangular carrier reaches its maximum (minimum) a measurement should take place. The next sampling will happen when the adjacent carrier reaches its minimum (maximum) if the number of carries is odd or at the crossing point of the two adjacent carries if the number of carriers is even.

The sampling instances at which a capacitor voltage can be measured using the first method (direct measurement) are depicted in Fig. 5(c). Similarly, the capacitor voltages measurable using the second method (indirect measurement) for each sampling instance are shown in Fig. 5(d). As it can be seen, none of these methods can provide measurement with constant sampling frequency and the chance of measuring a capacitor voltage is limited to specific instances.

Conversely, using the proposed measurement strategy, measurements take place at each sampling instance as shown in Fig. 5(e). Here, as it can be seen for each carrier period, all the control variables are updated twice per carrier period, which provides the controller with a high resolution constant frequency feedback signal.

The generated ac voltage undergoes a short transient after each voltage step due to parasitic capacitances and induc-

TABLE I
PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Circuit Parameter	Value
Dc Bus Voltage, V_{dc}	200 V
FCs (C_1, C_2, C_3)	260 μF
Linear Load, RL	R=10 Ω, L= 6 mH
Carrier Frequency, f_s	500 Hz
Fundamental Frequency, f	50 Hz

tances. In the proposed measurement strategy the measurement happens at the center of pulse which allows sufficient time for the decay of transient oscillation. Hence, the measurement remains immune to these switching transients. However, when the pulse width is too narrow, there is not enough time for the output voltage to reach steady state before measurement. In this case, the measurement is not reliable and the measurement unit disregards it. When, no measurement is performed at a particular sampling instance, the previously measured capacitor voltages values are used in the control system. Similarly, in the over modulation region in which no pulse occurs in the output voltage, the previously measured capacitor voltages values are used. Since the resolution of the proposed capacitor voltages reconstruction method is high and the capacitor voltages cannot change abruptly, the assumption of using previously measured capacitor voltages does not deteriorate the performance of the system.

The chance of having a narrow pulse increases as the switching frequency increases. Similarly, if the number of converter levels increases the pulses become narrower. Therefore, even though the proposed method is, in theory, independent of the switching frequency and number of converter levels, in practice they will be limiting factors to achieve satisfactory performance.

It is worthwhile mentioning this limitation does not devaluate the proposed measurement strategy compared to the previously discussed methods as they suffer from the same limitation.

IV. EXPERIMENTAL RESULTS

Experimental tests were performed on a low-power five-level FC converter. The circuit diagram of the converter prototype is shown in Fig. 6. The converter was controlled by a DSPACE 1006 with integrated DS 5203 FPGA board. The parameters of the converter are given in Table I.

The following three experiments were performed to compare the performance of the proposed single voltage sensor control system with the conventional one that uses as many voltage sensors as capacitors.

In the first experiment, initially, the capacitor voltage balancing method was deactivated and the voltages were regulated using natural PS-PWM. At time t_0, the proposed balancing method was activated to compensate the steady state error of the natural balancing and push the voltages towards the required reference values. The performance of the proposed single voltage sensor measurement method during this transient is shown in Fig. 7. As it can be seen, the proposed measurement method was able to track the actual values with

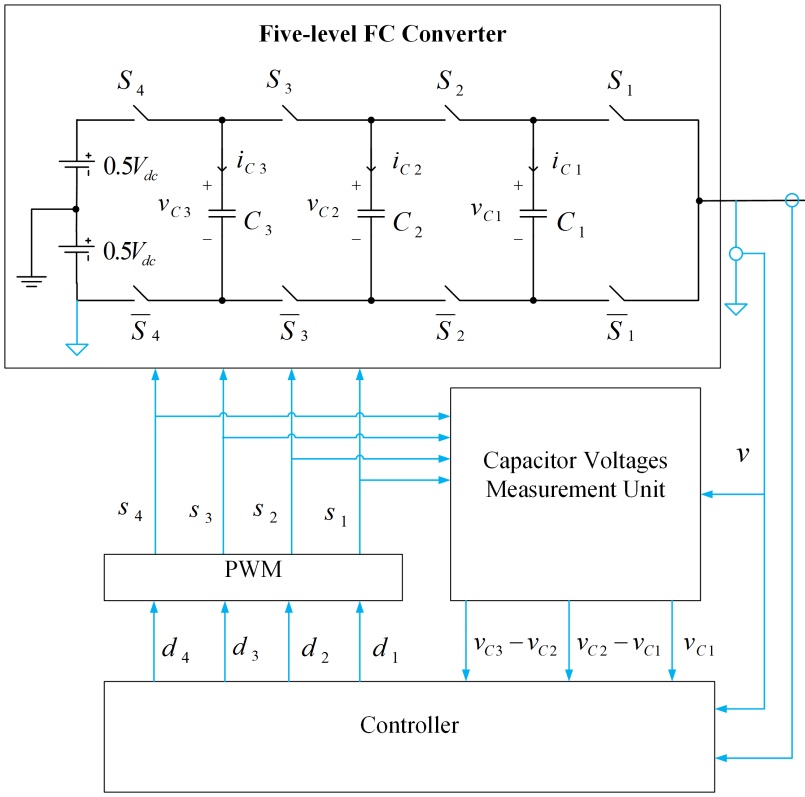

Fig. 6. Circuit diagram of the experimental system.

high accuracy. In this figure, the actual values of the signals were calculated using the measured capacitor voltages. The capacitor voltages were measured using individual voltage sensors at much higher frequency (10 kHz) to capture variations due to switching. As it can be seen from this figure, the reconstructed feedback signals using the proposed method remain within the tolerable error margin of the actual values. Similar to the actual values, the measured signals using the proposed method at twice the switching frequency, i.e. 1 kHz, contain higher order harmonics which need to go through a low pass filter before entering the voltage balancing loop. The 1 kHz sampling frequency using the proposed method is already twice the operating frequency of the discrete control system, which shows no estimation mechanism is needed and online measurement takes place at each step. The same test was performed using the conventional balancing method [27] in order to compare it with the proposed method. The capacitor voltages before and after activation of the voltage balancing are shown for the conventional and proposed balancing methods in Figs. 8(a) and (b), respectively. From these results, it can be concluded that with the proposed method the performance of the system does not deteriorate and remains comparable to the conventional method despite having a simpler structure and lower sensor count.

In the second experiment, the performance of the proposed method was tested against a sudden load transient. Initially, the converter was operated with the RL load given in Table I, then, at time t_0, the load was changed from $R = 10\Omega$ to $R = 20\Omega$. Fig. 9 shows the effectiveness of the proposed

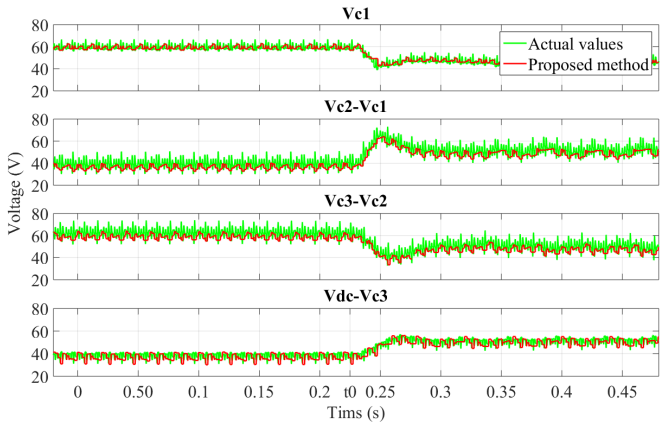

Fig. 7. Measured controllers' feedback signals using the proposed single voltage sensor method and using multiple voltage sensors (actual values) during a sudden balancing method activation test on the proposed control system.

single voltage sensor measurment method for this case. The dynamic performance of the proposed and conventional balancing method [27] is compared in Fig. 10(b). It can be seen that the proposed single voltage sensor method was able to regulate the capacitor voltages without any deterioration in the performance when compared with the conventional method.

In the last experiment, a step change in the amplitude of the ac voltage reference of the inverter from 0.9 p.u to 0.5 p.u was tested (base voltage, V_b=100 V). The converter was operating with the RL load given in Table I. At time t_0, the modulation index m was changed from 0.9 to 0.5. Fig. 11 shows that the proposed measurement method can follow the actual voltages during this transient. The dynamic performance of the proposed and conventional balancing method [27] is compared in Fig. 12(a) and (b), respectively. No deterioration in performance can be observed when the proposed method based on a single voltage sensor was used. The experiments showed that the proposed single voltage sensor measurement and balancing method has equivalent performance in regulating the capacitor voltages as the conventional one. Additional results in Fig. 13 show that the load current quality remains unaffected as well. Fig. 13(a) shows the harmonic content of the load current when the conventional method is used. Comparing this figure with Fig. 13(b), which shows the harmonic content of the load current using the proposed method, it can be seen that the total harmonic distortion and the location and amplitude of the significant harmonics remain almost the same.

V. Conclusion

This paper has proposed a new capacitor voltage measurement and balancing method for the FC converter, which allows effective operation when the capacitor voltage sensors are replaced with a single voltage sensor at the ac side. Effectiveness of the proposed method has been verified experimentally in a five-level FC converter prototype. The method is very simple to implement and can be applied to FC converters with different number of levels.

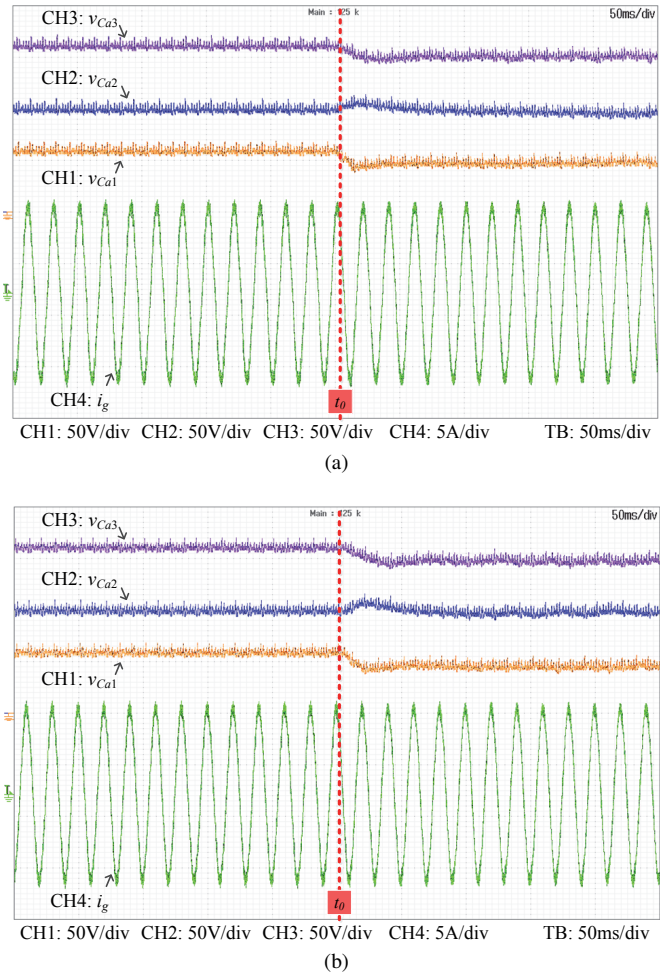

Fig. 8. Comparison of capacitor voltages when the voltage balancing is activated at t_0. (a) Conventional balancing method [27] and (b) proposed single voltage sensor balancing method.

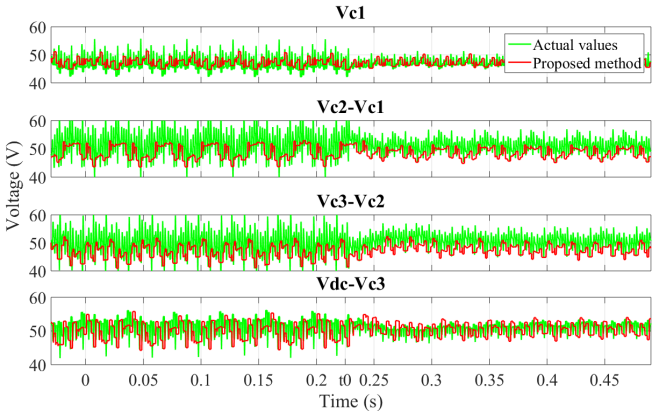

Fig. 9. Measured controllers' feedback signals using the proposed single voltage sensor measurement method and with multiple voltage sensors (actual values) during a step load change test on the proposed control system (load resistor suddenly changes from $R = 10\Omega$ to $R = 20\Omega$ at t_0).

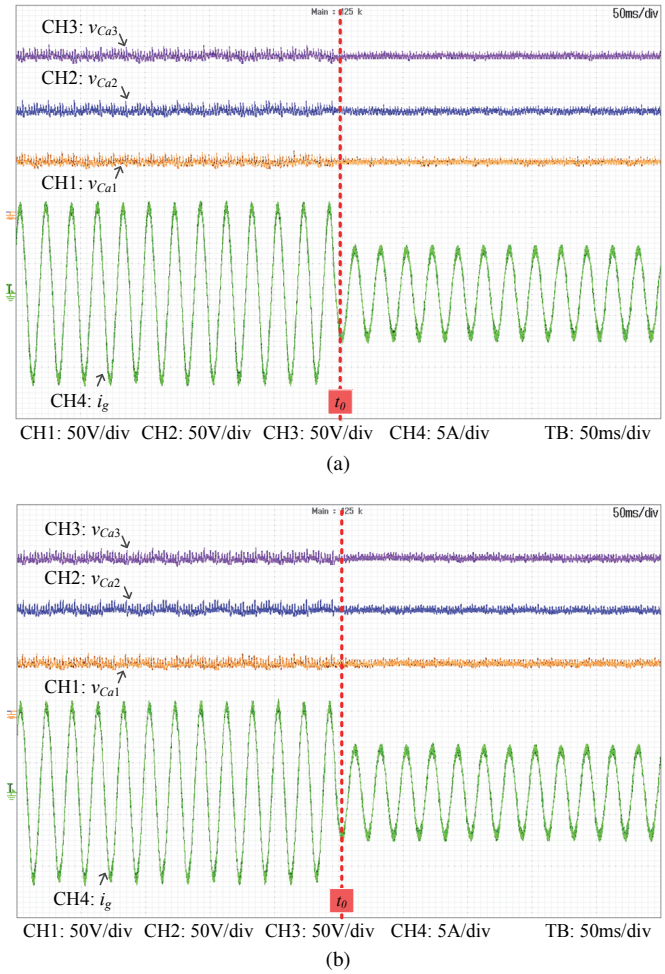

Fig. 10. Comparison of capacitor voltages during a step load change at t_0: (a) the conventional balancing method in [27] and (b) the proposed balancing method.

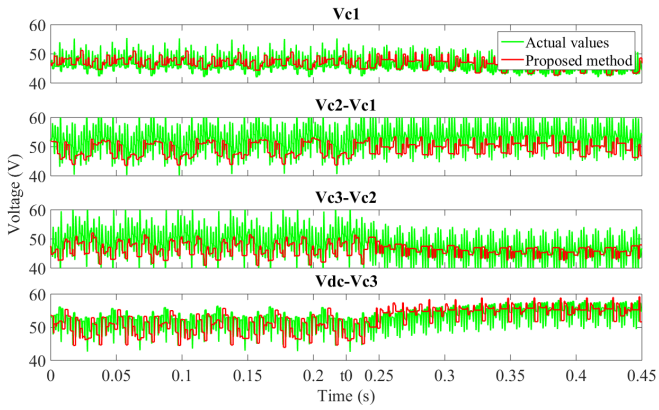

Fig. 11. Measured controllers' feedback signals using the proposed single voltage sensor measurement method and using multiple voltage sensors (actual values) during a step ac reference voltage change test on the proposed control system (modulation index suddenly changes from $m = 0.9$ to $m = 0.5$ at t_0).

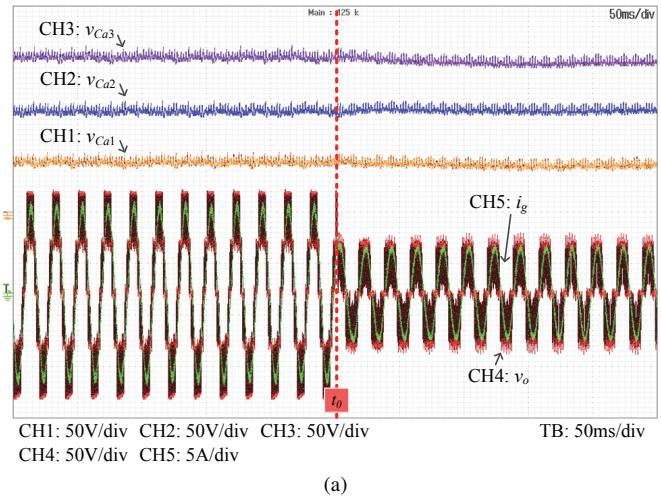

Fig. 12. Comparison of capacitor voltages during a step change in the ac reference voltage at t_0: (a) the conventional balancing method [27] and (b) the proposed balancing method.

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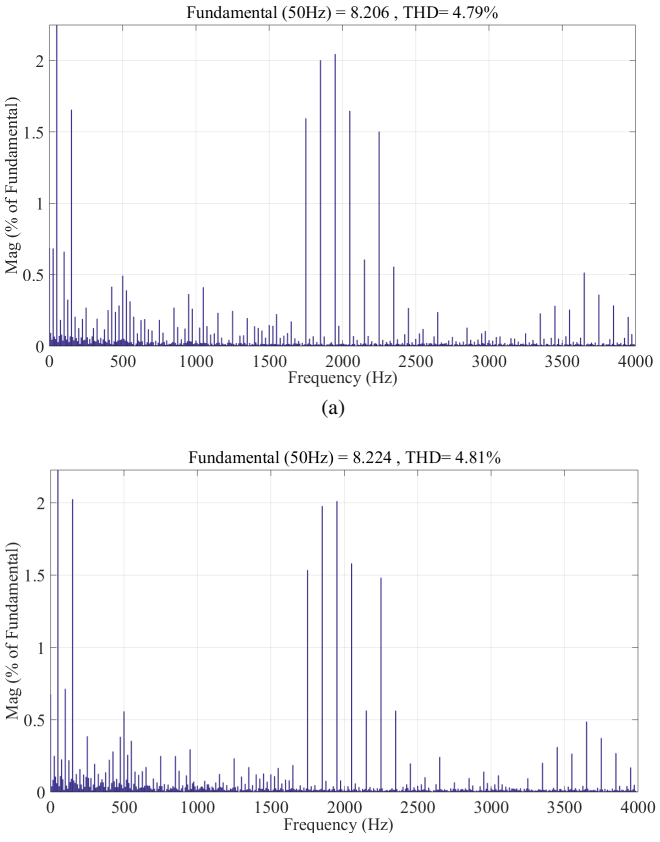

Fig. 13. (a) Load current harmonics using the conventional method [27] and (b) the proposed method.

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